

# SILICON WAFER AND SILICON EPITAXIAL WAFER AND PRODUCTION METHODS THEREFOR

**Patent number:** WO0225717

**Publication date:** 2002-03-28

**Inventor:** QU WEI FEIG [JP]; HAYAMIZU YOSHINORI [JP]; TAKENO HIROSHI [JP]

**Applicant:** SHINETSU HANDOTAI KK [JP]; QU WEI FEIG [JP]; HAYAMIZU YOSHINORI [JP]; TAKENO HIROSHI [JP]

**Classification:**

- **international:** H01L21/322

- **european:** C30B33/00; H01L21/322B8

**Application number:** WO2001JP08006 20010914

**Priority number(s):** JP20000286054 20000920

**Also published as:**

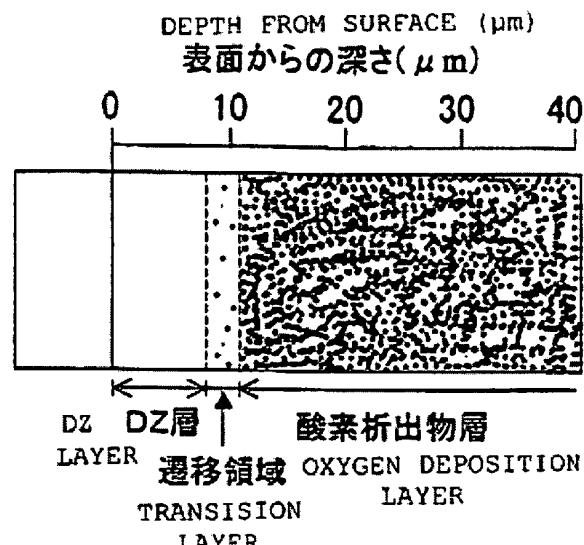
- [icon] EP1326270 (A1)
- [icon] US6858094 (B2)
- [icon] US2004005777 (A1)
- [icon] JP2002100631 (A)

**Cited documents:**

- [icon] US5961713
  - [icon] JP62202528
  - [icon] JP63090141
  - [icon] JP5058788
  - [icon] JP3185831
- [more >>](#)

## Abstract of WO0225717

A silicon wafer having a DZ layer in the vicinity of the surface thereof and an oxygen deposition layer in a bulk unit, wherein each of interstitial oxygen concentrations in the DZ layer, the oxygen deposition layer and in a transition layer between the DZ layer and the oxygen deposition layer is up to 8 ppm; a silicon epitaxial wafer having an epitaxial layer formed on the surface of this silicon wafer; and a production method of a silicon wafer, comprising the steps of growing a silicon single-crystal rod having an initial interstitial oxygen concentration of 10-25 ppm by a CZ method, processing the silicon single-crystal rod into a wafer, and subjecting the wafer to a first heat treating at 950-1050 DEG C for 2-5 hours, a second heat treating at 450-550 DEG C for 4-10 hours, a third heat treating at 750-850 DEG C for 2-8 hours, and a fourth heat treating at 950-1100 DEG C for 8-24 hours, whereby providing the production method of a silicon wafer capable of ensuring a high resistivity despite a device production heat treating.



Data supplied from the esp@cenet database - Worldwide